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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/853,111	05/10/2001	Salman Akram	MICT-0012-D1-US (97-0141)	7172

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TROP PRUNER & HU, PC
8554 KATY FREEWAY
SUITE 100
HOUSTON, TX 77024

EXAMINER

CHAMBLISS, ALONZO

ART UNIT	PAPER NUMBER
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2827

DATE MAILED: 07/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/583,111

Applicant(s)

BARTH ET AL.

Examiner

Alonzo Chambliss

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 5/6/02(amendment C).
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 15-22 and 32-35 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 15-22 and 32-35 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on 18 February 2002 is: a) ☒ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No: _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

1. Amendment C filed on 5/6/02 has been fully considered and made of record in Paper No. 5.

Response to Arguments

2. Applicant's arguments with respect to claims 15-22 and 32-35 in Paper No.5 has been considered but are moot in view of the new ground(s) of rejection. The previous non-final rejection filed on 4/3/02 in Paper No. 4 is withdrawn. Therefore, this action is made **non-final**.

Drawings

3. The corrected or substitute drawings were received on 2/28/02. These drawings are approved by the examiner. However, new formal drawings are required in this application because the corrected drawings received on 2/28/02 have the correction made in red ink instead of black ink. Applicant is advised to employ the services of a competent patent draftsman outside the Office, as the Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 15-22 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Klink et al. (U.S. 5,227,995).

With respect to Claim 15, Klink teaches stacking at least two semiconductor dies 8, 10 having substantially the same rectangular dimensions on top of one another such that one of the dies 10 is mounted on top of the lead frame fingers 16 (i.e. inner leads of the lead frame 14) and the other of the dies 10 is mounted on the die 10 mounted on the die mounted on the lead frame fingers 16. Each of the dies 8, 10 are wire bonded to the lead frame 14 (see col. 1 lines 54-57; Fig. 4). Giving the teachings of the above process steps, claim 15 is clearly anticipated by Klink.

With respect to Claim 16, Klink teaches that one of the semiconductor dies 10 is mounted on the back to back on the other semiconductor die 8 (see col. 2 lines 67 and 68 and col. 3 line 1; Fig. 4). Giving the teachings of the above process steps, claim 16 is clearly anticipated by Klink.

With respect to Claim 17, Klink teaches that one of the semiconductor dies 10 is adhered to the other of the semiconductor dies 8 by an adhesive layer (see col. 3 lines 1-4). Giving the teachings of the above process steps, claim 17 is clearly anticipated by Klink.

With respect to Claim 18, Klink teaches a first die 10 has a lead on chip configuration (i.e. when a lead is attached on the surface of the chip) as seen in Fig. 4. Giving the teachings of the above process steps, claim 18 is clearly anticipated by Klink.

With respect to Claim 19, Klink teaches a semiconductor die 10 secured to the lead frame 14 and the other of the dies 8 is secured to the die secured to the lead frame 14 (see Fig. 4). Giving the teachings of the above process steps, claim 19 is clearly anticipated by Klink.

With respect to Claim 20, Klink teaches semiconductor dies 8, 10 are wire bonded to the lead frame 14, wherein the dies 8, 10 have facing sides and outwardly facing sides by extending wire to bond pads 26, 28 on the outwardly facing sides of the dies (see Fig. 4). The outwardly facing sides are the sides that are facing towards the end portions 16, respectively. Giving the teachings of the above process steps, claim 20 is clearly anticipated by Klink.

With respect to Claim 21, Klink teaches locating a first semiconductor die 10 on the lead fingers 16 (i.e. inner leads of lead frame 14). A second semiconductor die 8 is stacked on the first semiconductor die 10. Bonding pads 26, 28 (i.e. power and ground supply leads) of the semiconductor dies 8, 10 are electrically connected to lead fingers 16 of the lead frame 24, respectively (see col. 2 lines 41-62; Fig. 4). Giving the teachings of the above process steps, claim 21 is clearly anticipated by Klink.

With respect to Claim 22, Klink teaches encapsulating the semiconductor dies 8, 10 and the lead frame 14 in a single package body 4 (i.e. housing) (see col. 2 lines 22-40; Fig. 4). Giving the teachings of the above process steps, claim 22 is clearly anticipated by Klink.

6. Claims 32-35 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Kohno et al. (U.S. 5,347,429).

With respect to Claim 32, Kohno teaches stacking first and second semiconductor dies 8, 10 having substantially the same rectangular dimensions on top of one another. The first semiconductor die 1 is mounting on the lead frame 4, since the first semiconductor die 1 is mounted on leads 4L that are apart of lead frame 4. The second semiconductor die 2 is mounted only on the first semiconductor die 2 (see col. 3 lines 27-42; Fig. 2). Giving the teachings of the above process steps, claim 32 is clearly anticipated by Kohno.

With respect to Claim 33, Kohno teaches wire bonding (i.e. using wires 5 to create a bond between the dies and the lead frame) the first and second semiconductor dies 1, 2 to the lead frame 4 (see col. 3 lines 32-42; Fig. 4). Giving the teachings of the above process steps, claim 33 is clearly anticipated by Kohno.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 34 and 35 rejected under 35 U.S.C. 103(a) as being unpatentable over Kohno et al. (U.S. 5,347,429) as applied to claim 33 above, and further in view of Klink et al. (U.S. 5,227,995).

Kohno fails to disclose two processing steps:

(1) a first semiconductor die that is mounted back to back on the second semiconductor die;

(2) one of the semiconductor dies adhered to the other of the semiconductor dies by an adhesive layer.

However, with respect to Claim 34, Klink discloses that a first semiconductor die 10 is mounted on the back to back to a second semiconductor die 8 (see col. 2 lines 67 and 68 and col. 3 line 1; Fig. 4). Kohno and Klink have substantially the same environment, since both Kohno and Klink disclose a first and second semiconductor dies mounted to each other, wherein the first die is attached to a lead frame and the first and second semiconductor dies and lead frame are encapsulated in a single package body. Therefore, it would have been obvious to one skilled in the art to substitute the back to back configuration between a first and second semiconductor dies with the process of Kohno, since the back to back configuration of the first and second semiconductor dies is an alternate process of attaching two semiconductor dies together as taught by Klink.

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With respect to Claim 35, Klink discloses that one of the semiconductor dies 10 is adhered to the other of the semiconductor dies 8 by an adhesive layer (see col. 3 lines 1-4).

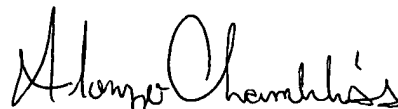
The prior art made of record and not relied upon is cited primarily to show the process of the instant invention.

Conclusion

9. Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (703) 306-9143. The fax phone number for this Group is (703) 308-7722 or 7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-7956.

AC/July 3, 2002


Alonzo Chambliss
Examiner
Art Unit 2827